**Lab 02**

**Objectives:**

This lab will enable students to:

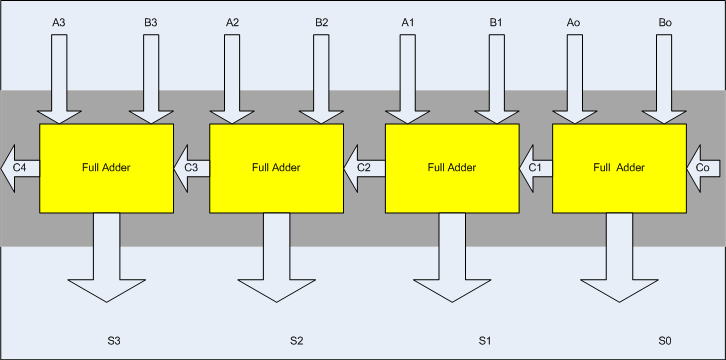
* + Learn top down and bottom up design methodologies
  + Data flow level modeling

**TASK 1:**

**4 bit Ripple Carry Adder**

**Block Diagram:**

Following is the block diagram of a 4 bit Ripple Carry Adder.

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**Steps for task 1a:**

The following steps should be performed while designing a 4 bit RCA adder

**ModelSim:**

1. First implement a Full adder using data gate level modeling.
2. Simulate the Full adder with a test bench.
3. Instantiate the Full adder four times and connect the circuit as shown.
4. Now again write a test bench and simulate the 4 bit RCA.

**Task 1b:**

Design the 4 bit full adder using data flow level modeling.